WHAT IS CLAIMED IS:

1. A circuit comprising:

a comparator;

a flip flop coupled to an output of the comparator;

a fixed off time/counter unit (FOTCU) coupled to the flip flop, the FOTCU containing circuitry to generate a signal for a specified amount of time and to reset itself once the specified amount of time expires; and

a gate having a first input coupled to the FOTCU and a second input coupled to an output of the comparator, the gate to control the propagation of the output of the comparator when a signal generated by the FOTCU is in a first state.

2. The circuit of claim 1, wherein the flip flop comprises an S-R flip flop, and wherein the output of the comparator is coupled to an S input of the flip flop.

3. The circuit of claim 1, wherein the FOTCU has as an input a reference clock operating at a known frequency, and wherein, when the flip flop asserts an active signal value on its output, the FOTCU begins to generate the signal.

4. The circuit of claim 3, wherein, after the specified amount of time expires, the FOTCU asserts an active signal on a finish signal line to clear the flip flop, and wherein when the flip flop is cleared, the FOTCU stops generating the signal.

5. The circuit of claim 4, wherein the flip flop comprises an S-R flip flop, and wherein the finish signal line is coupled to a R input of the flip flop.

6. The circuit of claim 1, wherein the gate comprises a negative-or (NOR) logic gate.

7. The circuit of claim 1, wherein the FOTCU counts a number of clock pulses to determine the expiration of the specified amount of time.

8. A hysteretic controlled switch regulator comprising:

a switch and filter unit (SFU) having an input coupled to an input voltage and an output coupled to a load, the SFU containing circuitry to convert a direct current (DC) voltage with ripple into a stable DC output voltage;

a comparator coupled to the SFU, the comparator to compare an output voltage generated by the SFU with a reference voltage; and

a fixed off time unit (FOT) coupled to the comparator and the SFU, the FOT containing circuitry to affect the operation of the SFU.

9. The hysteretic controlled switch regulator of claim 8, wherein the FOT comprises:

a flip flop coupled to an output of the comparator;

a fixed off time/counter unit (FOTCU) coupled to the flip flop, the FOTCU containing circuitry to generate a signal for a specified amount of time and to reset itself once the specified amount of time expires; and

a gate having a first input coupled to the FOTCU and a second input coupled to an output of the comparator, the gate to control the propagation of the output of the comparator when the signal generated by the FOTCU is inactive.

10. The hysteretic controlled switch regulator of claim 9, wherein the signal generated by the FOTCU disables the conversion of the input voltage with ripple into the stable DC output voltage.

11. The hysteretic controlled switch regulator of claim 8, wherein the SFU comprises:

a switch coupled to the input voltage, the switch to enable the conversion of the input voltage into the stable DC output voltage when closed; and

a filter coupled to the switch, the filter to eliminate high frequency components.

12. The hysteretic controlled switch regulator of claim 11, wherein the switch is an N-type metal oxide semiconductor (NMOS) transistor.

13. The hysteretic controlled switch regulator of claim 11, wherein the filter comprises a low-pass filter.

14. The hysteretic controlled switch regulator of claim 13, wherein the filter comprises:

an inductor having a first terminal coupled to the switch and a second terminal coupled to the load; and

a capacitor having a first terminal coupled to the second terminal of the inductor and a second terminal coupled to an electrical ground.

15. The hysteretic controlled switch regulator of claim 8, wherein the comparator asserts an active value on its output when the output voltage is greater than the reference voltage.

16. The hysteretic controlled switch regulator of claim 8, wherein when the SFU is enabled, the output voltage will rise until the output voltage exceeds the reference voltage, and wherein when the output voltage exceeds the reference voltage, the comparator asserts an active value on its output and the FOTCU generates a signal to disable the SFU.

17. The hysteretic controlled switch regulator of claim 16, wherein a magnitude of the load will determine how rapidly the output voltage rises.

18. The hysteretic controlled switch regulator of claim 17, wherein when the load is small in magnitude, the output voltage will rise slowly.

19. The hysteretic controlled switch regulator of claim 8, wherein the input voltage is a rectified voltage produced by an alternating current (AC) adaptor.